APPLICATION FOR U.S. LETTERS PATENT

TITLE:

REMOVING GROUND PLANE RESONANCE

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REMOVING GROUND PLANE RESONANCE

Field of the Invention

The present invention relates to printed circuit boards (PCBs). More particularly, the present invention relates to alterations in a PCB ground plane to remove resonance.

Background of the Invention

Printed circuit boards (PCBs) are widely used in the electronics and computer industries to mechanically and electrically couple individual components. A "motherboard" in a personal computer (PC), used to mount, and connect, a central processing unit (CPU) with other associated components is but one common example of a PCB. Generally, a PCB comprises a number of layers through which electrical signals may be routed, separated by dielectric layers. The layers for routing electrical signals may contain multiple (conducting) traces, each electrically isolated, or the entire layer may be electrically conductive. Conductive layers may be used to efficiently provide access to a particular voltage level, or voltage plane, over the entire area of the PCB. PCBs with on or more power planes, at voltages such as V_{dd}, and one or more ground planes are relatively common.

One design choice in routing signals within a PCB, is between routing on the top layer (microstrip routing) or routing in one of the inner layers (stripline routing). Microstrip routing typically provides faster signal speeds or "flight times" and microstrip routing, at the expense of requiring more complete

connections to the routing traces. Signal speeds of 153 ps/in for microstrip routing and 170 ps/in for stripline routing are typical. An advantage of stipline routing is that such a routing makes it easier to electrically isolate the signals using isolation lines and ground planes.

The design of a trace, or conductor for a particular signal path, depends on many factors. Two important factors being the locations of the points to be connected and the required impedance of the trace. The required impedance will typically be set by the components connected by the trace, with the actual impedance a function of the inductance and capacitance of the particular trace design. Eventually, the length, width, and geometry of the trace are defined for an acceptable signal routing scheme. However, there are combinations of clock speeds and signal values that degrade the quality of signal transmissions for a given signal routing scheme. Resources within a PCB may occur when a signal on a single signal path, although isolated from other signals on the PCB, oscillates at, or near, an integer multiple of signal transit time. Such resonance may seriously degrade the performance of the PCB.

Figure 1 depicts the stripline routing of traces 2 within a single layer of a PCB 4. The routing shown in Figure 1 may be used within a RAMBUS RIMM module containing dynamic random access memory (DRAM) devices, RDRAMs, as licensed by Rambus, Inc. of Mountain View, California. The signal routing in Figure 1 does not reflect an embodiment of the present invention. This signal routing may be susceptible to resonance under certain conditions.

Although the present invention is not intended to be limited to any particular PCB 4, or trace 2 design, an embodiment of the present invention may be used to improve signal transmission characteristics in a device such as a

RDRAM. That is, under some combinations of clock speeds and signal values, resonance may decrease device performance and an embodiment of the present invention may be used to prevent, or reduce, the decrease in performance.

Summary of the Invention

A method and apparatus for decreasing resonance in a printed circuit board (PCB) uses cuts in a ground plane to slow a signal passing through the ground plane. Cuts in the ground plane may be used alone or in conjunction with the lengthening of signal traces.

Brief Description of the Drawings

Figure 1 shows signal trace routing within one layer of a PCB.

Figure 2 shows a detailed depiction of a signal trace within one layer of a PCB together with grounded isolation lines.

Figure 3 is a cross section through of a PCB showing the multiple layers.

Figure 4A-4B depicts two layouts of a signal trace or a PCB.

Figure 5 depicts a cut in a PCB ground plane in accordance with an embodiment of the present invention.

Figure 6 illustrates the details of a zipper cut pattern in accordance with an embodiment of the present invention.

Detailed Description

An embodiment of the present invention is directed to improving the signal transmission characteristics within a printed circuit board (PCB) by removing resonance from a ground plane.

An embodiment of the present invention will be described in the context of a RAMBUS RIMM module. The present invention is not, however, intended to be limited to any such particular application. Those of ordinary skill in the art will, with the benefit of the herein disclosure, be able to use the present invention in a wide variety of electronic devices where resonance may cause problems at certain clock speeds and/or with certain combinations of signal values.

In the design of traces 2 for high speed electronic devices, such as but, not limited to, PCB 4, great care is often taken to avoid interference with signals carried by traces 2. Figure 2, shows one such design that may be used to shield a signal carried by trace 2, it is an enlarged view of trace 2 on a layer of PCB 4. Trace 2 is a 18 mil wide conductor, that is located between two 5 mil wide insulators 6. Also bordering insulators 6, on each side of trace 2, are two 5 mil wide isolation lines 8. Isolation lines 8 are typically conductive and are preferably grounded to a single common ground. In a PCB 4, each of the signal traces 2 may be surrounded on the particular "horizontal" layer within PCB 4, by insulators 6 and isolation lines 8. In addition, signal trace 2 may be shielded vertically within PCB 4. Turning now to Figure 3, a cross section through a PCB, a particular layer 10 with traces 2, such as shown in Figure 1, makes up but one horizontal layer with a PCB 4. Above and below layer 10 may be dielectric layers 12 and ground planes 14. With such a design, trace 2 is surrounded both horizontally and vertically with a dielectric and a ground in

order to isolate trace 2 and to minimize the effects of other signals on the one carried by trace 2. There are, however, situations where such isolation alone is not effective, resulting in poor device performance, such as single bit errors. These problems and some solutions to them, will be further elaborated below.

One use of PCBs 4 is to allow standard configurations, such as a standard connect pin layout on a device, while using dissimilar component level devices to make up the device. A common example, known to those of ordinary skill in the art, would be single inline memory modules (SIMMs) such as a 72-pin SIMM specified by the Joint Electronic Device Engineering Council (JEDEC). Although many memory components, of varying sizes, may be used by various manufactures, the resulting device will "plug-in" to a standard 72-pin SIMM socket. Thus, the standardization of a particular PCB 4 layout, such as size and connection geometry, can be valuable. This is the case even though such a standard layout may not be "optimal" for each particular embodiment in design of performance.

The RAMBUS RIMM modules, while not eclipsing SIMMs in the total number of devices sold, have gained popularity and their geometry is somewhat "fixed" by the consistent use of that geometry. Even though the present geometry of an RAMBUS RIMM module may not be optimal for all situations, changing that geometry would incur costs.

The speed or transit times of signals to and from PCB 4 depend on the signal path, or traces 2, and the individual devices through which the signal will pass. A RAMBUS RIMM module type PCB 4 with 4 RDRAMs have a signal transit time of about 1.25 ns. For a 6 RDRAM configuration the transit time is about 1.4 ns. These times are essentially fixed for a given PCB 4 layout. High speed devices, such as a RAMBUS RIMM module, often have tight timing

budgets, such as a maximum skew between a clock and data signal of about 125ps. The layout of traces 2 in Figure 1 reflects such a tight timing budget. The lengths of the many traces 2 are equal, within approximately 10 mils, resulting in similar transit times over the various traces 2.

Most digital electronic devices use zeros and ones, corresponding to two different voltage levels, to represent data signals. In some data combinations, such as but not limited to, 01010101..., the signal oscillates between the two voltage levels. When, because of a particular clock speed and data combination, the voltage oscillation period nearly matches the transit times of signals through PCB 4, the resulting resonance may significantly decrease signal transmission performance.

Data is transferred by a RAMBUS RIMM module at 600 MHz, 712 MHz or 800 MHz, depending on the particular application. Unfortunately, these frequencies correspond to periods of 1.67 ns, 1.40 ns and 1.25 ns, respectively, which are close to some signal transit times. While not all data value combinations may lead to resonance, certain combinations might. For example, a string of zeros (or ones) may not cause a voltage switch, while the data string 00110011... may well cause problems because the data transfer rate might be an integer multiple of the voltage fluctuation rate. Because a device may see almost any combination of data values, it must be designed for the worst case.

The effect of resonance on signal performance is negative; it introduces instability. An embodiment of the present invention makes relatively small adjustments in the signal paths to avoid signal transit times near the data transfer rate in order to avoid resonance problems. That is, the two periods will preferably differ enough to avoid a resonance range. For example, increasing

the signal transit time for a 4 RDRAM RAMBUS RIMM module from 1.25 ns to 1.6 ns significantly decreases resonance related problems.

Preferably, the transit times of signals would differ from multiples of the period of the data transfer rate. One way to achieve this result, without altering the clock speed, is to change the lengths of traces 2 slightly to "detune" PCB 4. Figures 4A and 4B show one embodiment of lengthening traces 2. However, such lengthening of traces 2 does not directly effect resonance problems within a ground plane. In one case, detuning traces 2 still left the ground plane with a resonance caused fluctuation of approximately 100 mV. Eliminating such a fluctuation in the grand plane increases the signal-to-noise (S/N) ratio, which tends to decrease data transmission errors.

Electrical signals to and from any device typically require two conductors; typically a trace and a ground plane in PCB 4. Since a ground plane is typically a conductive layer of PCB 4, not individual traces 2, increasing the signal transit times through the ground plane requires different techniques than the lengthening used for traces 2. An embodiment of the present invention uses cuts in the conductive layer of a ground plane to reduce resonance and improve overall signal performance. Preferably, the cuts in a ground plane are coordinated with laying out and lengthening of traces 2.

Figure 5 illustrates a PCB 4 with cuts made to a ground plane, in accordance with an embodiment of the present invention. Traces 2 have been lengthened, similar to that shown in Figure 4B. The locations of ground plane cuts 16 are preferably coordinated with the locations of traces 2. Although only a single trace 2 layout is shown in Figure 5, the location of all traces 2 and ground plane cuts 16 or PCB 4 are preferably coordinated such that cuts 16 terminate at least 10 mils from an trace 2. In one embodiment of the present

invention, the locations of grand plane cuts 16 are similar in each grand plane layer within PCB 4. That is, cuts 16 are vertically aligned.

In one embodiment of the present invention, cut 16 is continuous. That is, there is almost no electrical current across cut 16. As is shown in Figure 5, cuts 16 are preferably made substantially perpendicular to the long axis of PCB 4. Another embodiment uses a non-continuous "zipper cut."

Figure 6 illustrates such a zipper cut pattern. Along the axis of cut 16, a series of approximately 10 mil long by 5 mil wide holes are created in the ground plane at a 20 mil spacings. The effect of a zipper cut pattern is a smaller decrease in signal transit times through a ground plane than a continuous cut 16 at the same location.